José L. Abellán, PhD - Assistant Professor - Résumé (November 2017)

Contact Information

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Research Interests

Broad Category: CPU/GPU/FPGA Architecture, Interconnection Network, Memory System, Silicon-Photonic Link Technology, Deep-Learning.
Specific Areas: General-Purpose GPU, Chip-Multiprocessor (CMP), APU System, Cache Coherence Protocol, Memory Consistency, HW/SW Synchronization, Network-on-Chip Design, HW/SW Acceleration for Deep-Learning, CMOS/Silicon-Photonic Technology, Thermal and Energy Management, 3D Stacked Architectures, Digital Circuits.

Education

Ph.D. Degree in Computer Science (2008-2012)

· **Academic Institution**: Facultad de Informática – University of Murcia (Spain).

· **Thesis**: *Efficient Synchronization and Communication in Many-Core CMPs.*
Date: December, 21st 2012.
Advisors: Dr. Manuel E. Acacio and Dr. Juan Fernández

M.S. Degree in Computer Science (2007-2008)

· **Academic Institution**: Facultad de Informática – University of Murcia (Spain).

· **M.S. Thesis**: *Planificación de Tareas y Balanceo de la Carga en el Cell BE.*
Advisors: Dr. Manuel E. Acacio and Dr. Juan Fernández.

B.S. Degree in Computer Engineering (2002-2007)

· **Academic Institution**: Facultad de Informática – University of Murcia (Spain).

· **Final Year Project**: *CellStats: Una herramienta para la evaluación de las operaciones básicas de sincronización y comunicación del Cell BE.*
Advisors: Dr. Manuel E. Acacio and Dr. Juan Fernández.

Honors and Awards

Education

1. Ph.D. Thesis: *Summa Cum Laude* qualification. December, 21st 2012.
2. B.S. Degree: Graduated with honors:
"Mención Honorífica a la Excelencia Académica". May, 15th 2008.

Research

1. Best Paper Award at the 25th IEEE International Parallel & Distributed Processing Symposium (IPDPS 2011).

Fellowships

Predoctoral Fellowship (January 2010 - April 2012)

· Beca Predoctoral de Formación del Personal Investigador.

· Granted by: Fundación Séneca (Región de Murcia) Agencia de Ciencia y Tecnología de la Región de Murcia (II PCTRM 2007-2010). Fellowship: 12461/FPI/09.

HiPEAC PhD student Collaboration Grant (June 2011 - September 2011)

· 4-months collaboration at the University of Ferrara (Italy).

· Granted by: HiPEAC (European Network of Excellence on High Performance and Embedded Architectures and Compilation).

Internships

Ferrara (Italy) (June 2011 - September 2011)

· **Institution**: "Dipartimento di Ingegneria" – University of Ferrara

· **Position**: Predoctoral Researcher

· **Advisor**: Assistant Professor Davide Bertozzi.

· **Duration**: 4 months.

Boston (USA) (October 2012 - August 2014)

· **Institution**: Electrical & Computing Engineering – Boston University

· **Position**: Postdoctoral Researcher

· **Advisor**: Assistant Professor Ajay Joshi.

· **Duration**: 23 months.

Books

1. José L. Abellán, Juan Fernández and Manuel E. Acacio. "Efficient and Scalable Manycores: Optimized Synchronization and Cache Coherency". ISBN: 978-3-659-37173-8. LAP Lambert Academic Publishing. March 2013.

Books Chapters

1. José L. Abellán, Juan Fernández and Manuel E. Acacio. "Efficient Hardware-Supported Synchronization Mechanisms for Manycores". ISBN: . Springer. August 2013.

Journal Publications

1. José L. Abellán, Juan Fernández and Manuel E. Acacio. "Characterizing the Basic Synchronization and Communication Operations in dual Cell-based blade through CellStats". *Journal of Supercomputing* [doi:10.1007/s11227-009-0292-7]. Vol. 53(2), pp. 247-268. August 2010.

2. José L. Abellán, Juan Fernández and Manuel E. Acacio. "Efficient Hardware Barrier Synchronization in Many-Core CMPs". *IEEE Transactions on Parallel and Distributed Systems.* [http://doi.ieeecomputersociety.org/10.1109/TPDS.2011.304]. Vol. 23(8), pp. 1453-1466. August 2012.

3. José L. Abellán, Juan Fernández and Manuel E. Acacio. "Design of an Efficient Communication Infrastructure for Highly-Contended Locks in Many-Core CMPs". *Journal of Parallel and Distributed Computing.*. Available online July, 3rd 2012. [http://dx.doi.org/10.1016/j.jpdc.2012.06.010].

4. José M. Cecilia, José L. Abellán, Juan Fernández, Manuel E. Acacio, José M. García and Manuel Ujaldón "Stencil Computations on Heterogeneous Platforms for the Jacobi Method: GPUs versus Cell BE". Journal of Supercomputing. [doi:10.1007/s11227-012-0749-y]. Vol. 62(2), pp. 787-803. November 2012.

5. Chao Chen, José L. Abellán and Ajay Joshi. "Managing Laser Power in Silicon-Photonic NoC Through Cache and NoC Reconfiguration". *IEEE Trans. on CAD of Integrated Circuits and Systems*. Vol. 34(6), pp. 972-985. June 2015.

6. Epifanio Gaona-Ramírez, José L. Abellán and Manuel E. Acacio. "Fast and efficient commits for Lazy-Lazy hardware transactional memory". *Journal of Supercomputing*. Vol. 71(12), pp. 4305-4326. December 2015.

7. Amir Ziabari, Yifan Sun, Yenai Ma, Dana Schaa, José L. Abellán, Rafael Ubal, John Kim, Ajay Joshi and David Kaeli, "UMH: A Hardware-based Unified Memory Hierarchy for Systems with Multiple Discrete GPUs". *JACM Transactions on Architecture and Code Optimization*. Vol. 13(4), pp. 35:1-35:25. December 2016.

8. José L. Abellán, Chao Chen and Ajay Joshi. "Electro-Photonic NoC Designs for Kilocore Systems". *ACM Journal on Emerging Technologies in Computing Systems*. Vol. 13(2), pp. 24:1-24:25. November 2016.

9. José L. Abellán, Ayse Coskun, Anjun Gu, Warren Jin, Ajay Joshi, Andrew Kahng, Jonathan Klamkin, Cristian Morales, John Recchio, Vaishnav Srinivas and Tiansheng Zhang "Adaptive Tuning of Photonic Devices in a Photonic NoC Through Dynamic Workload Allocation,". *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*. Vol. 36(5), pp. 801-814. May 2017.

10. José L. Abellán, Eduardo Padierna, Alberto Ros and Manuel E. Acacio. "Photonic-Based Express Coherence Notifications for Many-core CMPs". *Journal of Parallel and Distributed Computing. Accepted for publication.* [DOI].

International Conferences

1. José L. Abellán, Juan Fernández and Manuel E. Acacio. "CellStats: a Tool to Evaluate the Basic Synchronization and Communication Operations of the Cell BE". Proc. of the Euromicro Conference on Parallel, Distributed and Network-Based Processing (PDP 2008). Toulouse (France). February 2008.

2. José L. Abellán, Juan Fernández and Manuel E. Acacio. "Characterizing the Basic Synchronization and Communication Operations in Dual Cell based Blades". Proc. of the International Conference on Computational Science (ICCS 2008). Krakòw (Poland). June 2008.

3. Juan Fernández, Manuel E. Acacio, Gregorio Bernabé, José L. Abellán and Joaquín Franco. "Multicore Platforms for Scientific Computing: Cell BE and NVIDIA Tesla". Proc. of the Conference on Scientific Computing (CSC 2008). Las Vegas (NV-USA). July 2008.

4. José L. Abellán, Juan Fernández and Manuel E. Acacio. "A Novel Hardware-based Barrier Synchronization for Many-Core CMPs". Proc. of the Interconnection Network Architectures: On-Chip, Multi-Chip (INA-OCMC 2010). Pisa (Italy). January 2010.

5. José L. Abellán, Juan Fernández and Manuel E. Acacio. "Efficient and Scalable Barrier Synchronization for Many-Core CMPs". Proc. of the Computing Frontiers Conference (CF 2010). Bertinoro (Italy). May 2010.

6. José L. Abellán, Juan Fernández and Manuel E. Acacio. "A G-line-based Network for Fast and Efficient Barrier Synchronization in Many-Core CMPs". Proc. of the International Conference on Parallel Processing (ICPP 2010). San Diego (CA-USA). September 2010.

7. José L. Abellán, Juan Fernández and Manuel E. Acacio. "GLocks: Efficient Support for Highly-Contended Locks in Many-Core CMPs". Proc. of the 25th IEEE International Parallel & Distributed Processing Symposium (IPDPS 2011). Anchorage (Alaska-USA). May 2011. **BEST PAPER AWARD** in Architectures track.

8. José L. Abellán, Juan Fernández, Manuel E. Acacio, Daniele Bortolotti, Andrea Marongiu, Luca Benini and Davide Bertozzi. "Design of a Collective Communication Infrastructure for Barrier Synchronization in Cluster-Based Nanoscale MPSoCs". Proc. of the Design, Automaton & Test in Europe Conference (DATE 2012). Dresden (Germany). March 2012.

9. Epifanio Gaona, José L. Abellán, Manuel E. Acacio and Juan Fernández. "Deploying Hardware Locks to Improve Performance and Energy Efficiency of Hardware Transactional Memory". Proc. of the 26th International Conference on Architecture of Computing Systems (ARCS 2013). Prague (Czech Republic). February 2013.

10. José L. Abellán, Alberto Ros, Juan Fernández and Manuel E. Acacio. "Efficient Dir_0B Cache Coherency for Many-Core CMPs". Proc. of the International Conference on Computational Science (ICCS 2013). Barcelona (Spain). June 2013.

11. José L. Abellán, Alberto Ros, Juan Fernández and Manuel E. Acacio. "ECONO: Express Coherence Notifications for Many-Core CMPs". Proc. of the International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS 2013). Samos (Greece). July 2013.

12. Tiansheng Zhang, José L. Abellán, Ajay Joshi and Ayse K. Coskun. "Thermal Management of Manycore Systems with Silicon-Photonic Networks". Proc. of the Design, Automaton & Test in Europe Conference (DATE 2014). Dresden (Germany). March 2014.

13. Baldomero Imbernon, Antonio Llanes, Jorge Peña-García, José L. Abellán, Horacio Pérez Sánchez and José M. Cecilia. "Enhancing the Parallelization of Non-bonded Interactions Kernel for Virtual Screening on GPUs". Proc. of the International Work-Conference on Bioinformatics and Biomedical Engineering (IWBBIO 2015). Granada (Spain). April 2015.

14. Amir K. Ziabari, José L. Abellán, Rafael Ubal, Chao Chen, Ajay Joshi and David R. Kaeli. "Leveraging Silicon-Photonic NoC for Designing Scalable GPUs". Proc. of the 29th ACM on International Conference on Supercomputing (ICS 2015). California (USA). June 2015.

15. Amir K. Ziabari, José L. Abellán, Yenai Ma, Ajay Joshi and David R. Kaeli. "Asymmetric NoC Architectures for GPU Systems". Proc. of the 9th International Symposium on Networks-on-Chip (NOCS 2015). Vancouver (Canada). September 2015.

16. Fernando Pereñiguez-García and José L. Abellán. "Secure Communications in Wireless Network-on-Chips". Proc. of the 2nd International Workshop on Advanced Interconnect Solutions and Technologies for Emerging Computing Systems (AISTECS). Stockholm (Sweden). January 2017.

National Conferences

1. José L. Abellán, Juan Fernández and Manuel E. Acacio. "CellStats: una herramienta para la Evaluación de las Operaciones Básicas de Sincronización y Comunicación del Cell BE". Proc. of the XVIII Jornadas de Paralelismo. Zaragoza (Spain). September 2007.

2. José L. Abellán, Juan Fernández and Manuel E. Acacio. "CellSched: una Herramienta para Modelar Aplicaciones que Exhiben Paralelismo a Nivel de Bucle sobre el Cell Broadband Engine". Proc. of the XIX Jornadas de Paralelismo. Castellón (Spain). September 2008.

3. José L. Abellán, Juan Fernández and Manuel E. Acacio. "Efficient Hardware Support for Lock Synchronization in Many-core CMPs". Proc. of the XXII Jornadas de Paralelismo. Tenerife (Spain). September 2011.

4. José L. Abellán, Juan Fernández and Manuel E. Acacio. "Infraestructuras de Barrera Eficientes para Sistemas Clusterizados MPSoC". Proc. of the XXIII Jornadas de Paralelismo. Alicante (Spain). September 2012.

5. José L. Abellán, Eduardo Padierna, Alberto Ros and Manuel E. Acacio. "Manteniendo la Coherencia de Cachés con Tecnología Nanofotónica". Proc. of the XXVIII Jornadas de Paralelismo. Málaga (Spain). September 2017.

6. Antonio Llanes, José L. Abellán, Juan Gómez-Luna and José M. Cecilia. "Optimización del Algoritmo Ant Colony Optimization en sistemas Masivamente Paralelos". Proc. of the XXVIII Jornadas de Paralelismo. Málaga (Spain). September 2017.

Research Projects Participation

1. **Project**: "Arquitecturas Fiables y de Altas Prestaciones para Centros de Proceso de Datos y Servidores de Internet".
   Main Coordinator: José Duato, UPV, Spain
   Granted by: Spanish MEC, CSD2006-00046, years: 2006-2011.

2. **Project**: "Arquitecturas de Servidores, Aplicaciones y Servicios".
   Main Coordinator: José Manuel García Carrasco, UMU (José Duato, UPV), Spain
   Granted by: Spanish MEC, TIN2009-14475-C04, years: 2009-2012.

3. **Project**:"Electro-photonic NEtwork-on-chip Architectures in 1000+ Core systems (Program ID:W911NF-12-1-0211)".
   Main Coordinator: Ajay Joshi
   Granted by: DARPA, years: 2012-2014.

4. **Project**: "System-level Run-time Management Techniques for Energy-efficient Silicon-Photonic Manycore Systems (Program ID: CCF-1149549)".
   Main Coordinator: Ajay Joshi
   Granted by: DARPA, years: 2012-2014.

5. **Project**: "Leveraging Intra-chip/Inter-chip Silicon-Photonic Networks for Designing Next-Generation Accelerators (Program ID: 1525474)".
   Main Coordinator: Ajay Joshi
   Granted by: NSF, years: 2015-2018.

6. **Project**: "Desarrollo holístico de aplicaciones emergentes en sistemas heterogéneos".
   Main Coordinator: José María Cecilia and Andrés Muñoz (UCAM), Spain
   Granted by: Spanish MINECO, TIN2016-78799-P, years: 2016-2019.

Professional Activities

Reviewer of Journal Papers: IEEE Transactions on Parallel and Distributed Systems (2011, 2012, 2013). Journal of Supercomputing (2013, 2014, 2015, 2016). Transactions on Computer-Aided Design of Integrated Circuits and Systems (2014, 2017). Journal of Parallel and Distributed Computing (2015, 2016, 2017). ACM Transactions on Architecture and Code Optimization (2016, 2017). Journal of Lightwave Technology (2016, 2017).

TPC member: Euromicro Conference on Parallel, Distributed and Network-Based Processing (PDP 2014). Symposium on High-Performance Interconnects (HOTI 2014, 2017). Embedded and Ubiquitous Computing (EUC 2015). Workshop on General Purpose Processing Using GPUs (GPGPU 2014, 2015, 2016, 2017, 2018). Heterogeneous and Unconventional Cluster Architectures and Applications (HUCAA 2015). International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC 2015, 2016, 2017). International Conference on Networking, Architecture, and Storage (NAS 2015). International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD 2015). IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC 2016). 5th Workshop on Novel High Performance Computing algorithms and platforms in Bioinformatics (2017). 3rd International Workshop on Advanced Interconnect Solutions and Technologies for Emerging Computing Systems (AISTECS 2018). 5th High Performance Computing Conference (BASARIM 2017).

Program Chair: 2nd International Workshop on Advanced Interconnect Solutions and Technologies for Emerging Computing Systems (AISTECS 2017).

Workshop Chair: ACM International Conference on Computing Frontiers 2018 (CF 2018)

Track Chair: Track 4: Embedded Multicore/Manycore SoC Interconnection Networks. IEEE 12th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC-2018)

Session Chair: HiPEAC 2017: Session 7 (Caches).

Computer Skills

Operating Systems: Linux, Windows, Mac OS.

General-purpose Programing: C, C++, Java, Fortran, Pascal, Modula-2, Verilog.

Scripting Languages: Linux Shell, Python.

Parallel Programming: pthreads, MPI, OpenMP, OpenCL, Cell-SDK, CUDA, Cell-SuperScalar, Accelerated Library Framework (ALF), HSA ecosystem.

Experience with Simulators and Technical Tools: Cell-BE Performance Simulator, RSIM, Sim-PowerCMP, Virtutech Simics, GEMS, Graphite, Sniper, Multi2Sim, GEM5-apu, CACTI, McPAT, MATLAB, Inkscape, ROCm.

Experience with a Mainstream Industrial Synthesis Toolflow: Synopsys Physical Compiler, Cadence SoC Encounter and Synopsys PrimeTime.

Academic Experience

Assistant Professor (*Profesor Contratado Doctor por ANECA*)

- **Academic Institution**: Polytechnic Faculty – Catholic University of Murcia (Spain).
- **Courses**: September 2014 - now
  - Structure and Technology of Computers: 6 ECTS cr. + 6 ECTS cr. (online).
  - Software Quality: 4.5 ECTS cr. + 4.5 ECTS cr. (online).
  - Knowledge Engineering: 6 ECTS cr. + 6 ECTS cr. (online).
  - Advanced Visual Programming: 6 ECTS cr.

Teaching Assistant

- **Academic Institution**: Facultad de Informática – University of Murcia (Spain).
- **Courses**: February 2011 - June 2011
  - Structure and Technology of Computers: 6 ECTS cr.

Academic Training: Attendance to the "Fifth International Summer School on Advanced Architecture and Compilation for Embedded Systems (ACACES'09)". July, 12th-18th 2009.

Miscellaneous

Full Member of the HiPEAC European Network of Excellence.

IEEE Computer Society Member.